Layout Analysis – Analog Block Analysis

Sample Report
Analysis from an HD Video/Audio SoC
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1.1 Layout Analysis – Analog Block Analysis

This report provides an overview of an IC’s analog blocks. A lower level metal or polysilicon die photo is annotated to show the analog macrocells on the die. It provides an identification of the analog macrocells used on a chip, and the sizes of each. Clients use this information to compare to their own designs and determine if their competitors use different or smaller functional blocks. This helps to allocate research and development (R&D) resources and to determine when further analysis, such as circuit extraction, is warranted.

This report contains:

- Package photos
- Package X-ray
- Depot (bare die) die photo with die size measurements
- Die markings
- Annotated metal 1 or polysilicon die photo showing the major analog physical blocks on the die
- Zoomed-in views of each analog block on the Metal 1 or polysilicon layer
- Analog Block Measurements
- Discussion of possible functions of each analog block, including rationale
- Table summarizing the L, W, Area, and the % die area of each block
1 Overview

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2 Device Overview

2.1 Introduction

An overview of the major analog blocks and the types of RE required to complete the analysis (XXXX vs. public XXXX)

This report contains the following detailed information:

- Package photographs, package X-ray, die markings, die photograph, and die photographs with annotated analog blocks
- Measurements of horizontal dimensions of major microstructural features
- Identification of major analog blocks
- Description of analog blocks
- Higher magnification imaging of each analog block

All of the analysis for this report was performed on XXXX parts, with the following markings:

<table>
<thead>
<tr>
<th>Device</th>
<th>XXXX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package markings</td>
<td>XXXX</td>
</tr>
<tr>
<td>Die markings</td>
<td>XXXX</td>
</tr>
<tr>
<td>Date code</td>
<td>XXXX</td>
</tr>
</tbody>
</table>

Table 2.1.1 Device Identification
### 2.2 Device Summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manufacturer</td>
<td>XXXX</td>
</tr>
<tr>
<td>Foundry</td>
<td>XXXX</td>
</tr>
<tr>
<td>Part number</td>
<td>XXXX</td>
</tr>
<tr>
<td>Type</td>
<td>XXXX</td>
</tr>
<tr>
<td>Date code</td>
<td>XXXX</td>
</tr>
<tr>
<td>Package markings</td>
<td>XXXX</td>
</tr>
<tr>
<td></td>
<td>XXXX</td>
</tr>
<tr>
<td>Package type</td>
<td>XXXX</td>
</tr>
<tr>
<td>Package dimensions</td>
<td>XXXX</td>
</tr>
<tr>
<td>Die markings</td>
<td>XXXX</td>
</tr>
<tr>
<td></td>
<td>XXXX</td>
</tr>
<tr>
<td>Die size (die edge seal)</td>
<td>XXXX</td>
</tr>
</tbody>
</table>

Table 2.2.1 Device Summary
3 Device Identification

3.1 Package

Top and Bottom photographs of the XXXX package are shown in Figure 3.1.1 and Figure 3.1.2. The 976 pin micro ball grid array (BGA) package is 35 mm x 35 mm. The package markings include:

    XXXX
    XXXX

![Figure 3.1.1 Package Top](image_url)
Figure 3.1.2 Package Bottom
A plan view X-ray photograph is shown in Figure 3.1.3. The XXXX die was flip-chip mounted on the PCB of the XXXX package.

Figure 3.1.3 Package X-Ray
3.2 Die

Figure 3.2.1 shows a photograph of the XXXX die. The die is 9.02 mm x 7.84 mm as measured from the die seals, or 9.07 mm x 7.89 mm for the whole die. This yields a die area of 70.7 mm² within the die seals. Bond pads are arranged in a grid across the surface of the die.

Figure 3.2.1 Die Photograph
The die markings are shown in Figure 3.2.2 and Figure 3.2.3. These include:

XXXX
XXXX

Figure 3.2.2 Die Markings A

Figure 3.2.3 Die Markings B
4 Analog Functional Analysis

4.1 Analog Functional Block Analysis

The XXXX is a high performance, high definition (HD) satellite, cable, and IP set-top box DVR system-on-a-chip (SOC) solution designed for the next generation STBs.

This device builds upon the XXXX advanced HD video compression solutions by utilizing 65 nanometer process technology to significantly reduce bill of materials (BOM) costs, and enable higher levels of integration and system performance versus currently available solutions. As a result, equipment manufacturers can build next generation HD digital broadcast and IP set-top boxes supporting the latest interactive features, a wide range of video compression standards and networked personal video recorder (PVR) functionality.

Figure 4.1.1 shows the distinguishable analog functional blocks annotated on a photograph of the XXXX die, delayered to the metal 1 layer. The eleven analog blocks occupy 7.34 mm$^2$, or 10.26% of the die area.

Analog block AN 1 is the RF mod out circuit. Analog blocks AN 2 and AN 3 represent the six video DACs and audio DACs of this device. Analog block AN 4 is the HDMI. Analog block AN 5 is the Ethernet controller. Analog block AN 6 is the three USB transceivers. Analog block AN 7 is the DDR PLL of the DRAM controller. Analog block AN 8 appears to be a tuner circuit due to the presence of an inductor. Analog blocks AN 9 and AN 10 appear to be the clock generating circuitry of this device in the form of an internal oscillator and several PLLs. Analog block AN 11 is the SATA block.
Figure 4.1.1 Annotated Die Photograph – Analog Blocks
4.2 Analog Block Measurements

Table 4.2.1 shows the measurements of each analog block shown in Figure 4.1.1. Together, all the analog blocks occupy 7.34 mm², or 10.26% of the die.

<table>
<thead>
<tr>
<th>Analog Block</th>
<th>Possible Function</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Area (mm²)</th>
<th>Percentage of Die (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AN 1</td>
<td>RF Mod Out</td>
<td>0.51</td>
<td>0.73</td>
<td>0.37</td>
<td>0.52</td>
</tr>
<tr>
<td>AN 2</td>
<td>6 Video DACs</td>
<td>0.53</td>
<td>2.1</td>
<td>1.11</td>
<td>1.56</td>
</tr>
<tr>
<td>AN 3</td>
<td>Audio DAC(s)</td>
<td>1.18</td>
<td>0.38</td>
<td>0.45</td>
<td>0.63</td>
</tr>
<tr>
<td>AN 4</td>
<td>HDMI</td>
<td>0.48</td>
<td>1.12</td>
<td>0.54</td>
<td>0.75</td>
</tr>
<tr>
<td>AN 5</td>
<td>Ethernet</td>
<td>1.00</td>
<td>0.83</td>
<td>0.83</td>
<td>1.16</td>
</tr>
<tr>
<td>AN 6</td>
<td>USB transceivers</td>
<td>1.03</td>
<td>1.18</td>
<td>1.21</td>
<td>1.69</td>
</tr>
<tr>
<td>AN 7</td>
<td>DDR PLL</td>
<td>0.43</td>
<td>0.74</td>
<td>0.32</td>
<td>0.45</td>
</tr>
<tr>
<td>AN 8</td>
<td>Tuner</td>
<td>0.63</td>
<td>0.91</td>
<td>0.57</td>
<td>0.80</td>
</tr>
<tr>
<td>AN 9</td>
<td>Oscillator</td>
<td>0.36</td>
<td>0.41</td>
<td>0.15</td>
<td>0.21</td>
</tr>
<tr>
<td>AN 10</td>
<td>PLLs</td>
<td>Irregular</td>
<td>–</td>
<td>1.19</td>
<td>1.66</td>
</tr>
<tr>
<td>AN 11</td>
<td>SATA</td>
<td>1.18</td>
<td>0.51</td>
<td>0.60</td>
<td>0.84</td>
</tr>
<tr>
<td>Analog sum</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>7.34</td>
<td>10.26</td>
</tr>
<tr>
<td>All other</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>89.73</td>
</tr>
<tr>
<td>Die</td>
<td>–</td>
<td>7.89</td>
<td>9.07</td>
<td>71.56</td>
<td>100</td>
</tr>
</tbody>
</table>

Table 4.2.1 Analog Block Measurements
4.3 Plan View and Functional Analysis

This section contains optical microscope plan-view images of each of the eleven analog blocks listed in Table 4.2.1. The images are shown on the metal 1 layer.

Figure 4.3.1 is a plan-view image of the analog block AN 1, which is also the functional block BLK 1. Analog block A1 appears to be the RF mod out circuit.

Figure 4.3.1 Analog Block AN 1 – Metal 1
Figure 4.3.2 and Figure 4.3.3 are plan-view images of the analog block AN 2, which is also the functional block BLK 2. Analog block AN 2 represents the six video DACs of this XXXX device.
Figure 4.3.4 is a plan-view image of the analog block AN 3, which is also the functional block BLK 3. Analog block AN 3 represents the audio DACs of this XXXX device. Unlike analog block AN 2, where each stereo channel has its own DAC circuit, it appears that the two audio channels of analog block AN 3 are sharing one DAC circuit.
Figure 4.3.5 is a plan-view image of the analog block AN 4, which is located in the functional block BLK 4. Analog block AN 4 represents the HDMI interface of this XXXX device. Microscope inspection suggests that there are two pairs of differential channels. A bandgap voltage reference circuit also appears to be part of this block.
Figure 4.3.6 is a plan-view image of the analog block AN 5, which is located in the functional block BLK 5. This analog block AN 5 is the Ethernet controller interface of this XXXX device.

Figure 4.3.6 Analog Block AN 5 – Metal 1
Figure 4.3.7 is a plan-view image of the analog block AN 6, which is located in the functional block BLK 6. Analog block AN 6 represents the three USB transceivers of this device. The leftmost side of analog block AN 6 appears to be the voltage reference circuit.
Figure 4.3.8 is a plan-view image of the analog block AN 7, which is also the functional block BLK 8. Analog block AN 7 is possibly the DDR PLL of this XXXX device, which supplies the clock signals to the DDR2 interface and DRAM controller. The appearance of big capacitors and resistors indicate the filter part of the PLL.
Figure 4.3.9 is a plan-view image of the analog block AN 8, which is located in the functional block BLK 15. Analog block AN 8 appears to be the tuner circuit, based on microscope inspection and the appearance of the inductor.
Figure 4.3.10 is a plan-view image of the analog block AN 9, which is also the functional block BLK 16. Analog block AN 9 is possibly the oscillator circuit, based on its proximity to the crystal oscillator on the main PCB board and internal PLL circuits.
Figure 4.3.11 is a plan-view image of the analog block AN 10, which is located in the functional block BLK 17. In analog block AN 10 are the PLL circuits that supply the reference clock signals to the rest of the circuits of this XXXX device. Similar capacitors and resistors that were found on analog block AN 7 DDR PLL were also found on this block.
Figure 4.3.12 Analog Block AN 10, Right Side – Metal 1
Figure 4.3.13 is a plan-view image of the analog block AN 11, which is also the functional block BLK 18. Analog block AN 11 is the SATA interface/controller of this XXXX device.
5 Statement of Measurement Uncertainty and Scope Variation

Statement of Measurement Uncertainty

Chipworks calibrates length measurements on its scanning electron microscopes (SEM), transmission electron microscope (TEM), and optical microscopes, using measurement standards that are traceable to the International System of Units (SI).

Our SEM/TEM cross-calibration standard was calibrated at the National Physical Laboratory (NPL) in the UK (Report Reference LR0304/E06050342/SEM4/190). This standard has a 146 ± 2 nm (± 1.4%) pitch, as certified by NPL. Chipworks regularly verifies that its SEM and TEM are calibrated to within ± 2% of this standard, over the full magnification ranges used. Fluctuations in the tool performance, coupled with variability in sample preparation, and random errors introduced during analyses of the micrographs, yield an expanded uncertainty of about ± 5%.

The materials analysis reported in Chipworks reports is normally limited to approximate elemental composition, rather than stoichiometry, since calibration of our SEM and TEM based methods is not feasible. Chipworks will typically abbreviate, using only the elemental symbols, rather than full chemical formulae, usually starting with silicon or the metallic element, then in approximate order of decreasing atomic % (when known). Elemental labels on energy dispersive X-ray spectra (EDS) will be colored red for spurious peaks (elements not originally in sample). Elemental labels in blue correspond to interference from adjacent layers. Secondary ion mass spectrometry (SIMS) data may be calibrated for certain dopant elements, provided suitable standards were available.

A stage micrometer, calibrated at the National Research Council of Canada (CNRC) (Report Reference LS-2005-0010), is used to calibrate Chipworks’ optical microscopes. This standard has an expanded uncertainty of 0.3 µm for the stage micrometer’s 100 µm pitch lines. Random errors, during analyses of optical micrographs, yield an expanded uncertainty of approximately ± 5% to the measurements.

Statement of Scope Variation

Due to the nature of reverse engineering, there is a possibility of minor content variation in Chipworks’ standard reports. Chipworks has a defined table of contents for each standard report type. At a minimum, the defined content will be included in the report. However, depending on the nature of the analysis, additional information may be provided in a report, as value-added material for our customers.
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