

A grey L-shaped graphic consisting of a horizontal bar on top and a vertical bar on the left side, forming a corner.

Product Brief

Intel 14 nm Generation Tri-Gate Core M-5Y10 Broadwell Processor Technical Analysis Reports

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October 2014

Overview

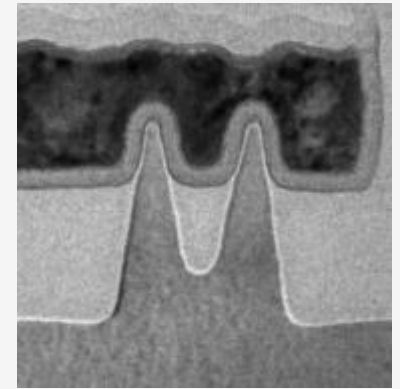
Chipworks has procured Intel 14 nm generation chips and technical analysis is underway.

The following technical analysis reports are in progress with **preliminary SEM and TEM analysis results** scheduled to be delivered to report pre-purchasers:

- Digital Library Functional Analysis Report (DLF-1410-801)
- Package Analysis Report (PKG-1409-801)
- Transistor Characterization Report (TCR-1409-801)
- Structural Analysis Report (SAR-1409-801)

Intel 14 nm Tri-Gate Background

- Intel's 14 nm technology is now qualified and in volume production
- This technology uses 2nd generation Tri-gate (Tri-Gate) transistors with industry-leading performance, power, density and cost per transistor
- The lead 14 nm product is a family of processors using the new Broadwell microarchitecture
- Intel's 14 nm technology will be used to manufacture a wide range of products, from high performance to low power



22 nm 1st Generation Tri-gate Transistor

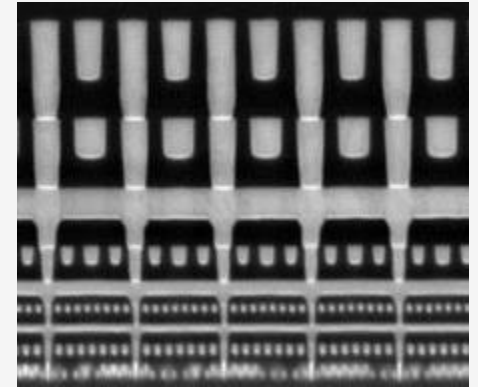


14 nm 2nd Generation Tri-gate Transistor

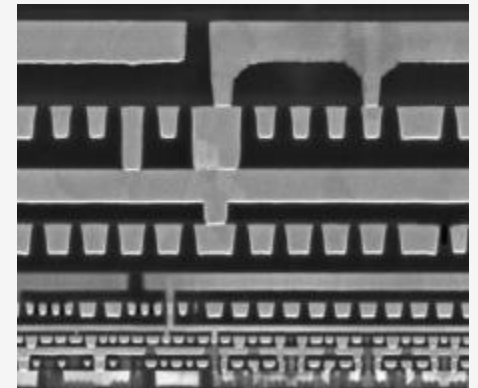
Source: http://download.intel.com/newsroom/kits/14nm/pdfs/Intel_14nm_New_uArch.pdf

Intel 14 nm Tri-Gate Background (cont.)

- Enables $\leq 9\text{mm}$ Fanless 2-in-1's for the First Time on the Intel Core™ Roadmap
- Greater than 2X reduction in TDP with better performance vs. Haswell-Y
- 50% Smaller Package (XY), 30% Thinner
- 60% Lower SOC Idle Power for Increased Battery Life



22 nm Generation:
80 nm metal pitch



14 nm Generation:
52 nm (0.65x)
minimum pitch

Source: http://download.intel.com/newsroom/kits/14nm/pdfs/Intel_14nm_New_uArch.pdf

List of reports

Chipworks Report	Date	Links
Digital Library Functional Analysis Report (FAR-1410-801)	Early 2015	
<ul style="list-style-type: none"> SEM images of layout over polysilicon and all metal layers using a bevel sample Statistical measurements of digital logic implemented in major logic libraries: Primary functional cells · P/N ratio · Area percentage utilization Gross and actual density · Track height · Filler cells · Power connections 		Chipworks E-Store »
Package Analysis Report (PKG-1409-801)	Mid December	
<ul style="list-style-type: none"> Device overview including ball count, package mass, heat sink, mass, lid mass and more Optical and SEM images of the cross section SEM EDS for materials analysis Observed critical dimensions 		Example Report »
		Chipworks E-Store »
Transistor Characterization Report (TCR-1409-801)	Mid December	
<ul style="list-style-type: none"> All transistor and transfer characteristics Transconductance curves and the body effect parameter Output and punchthrough characteristics Gate oxide leakage currents 		Example Table of Contents »
		Chipworks E-Store »
Structural Analysis Report (SAR-1409-801)	Mid December	
<ul style="list-style-type: none"> Package overview including a package x-ray Die photograph identifying location of memory blocks Top-down layer-by-layer analysis of the back end processing Analysis of the front end processing including SEM and TEM imaging Memory cell analysis Layout – detailed SEM and optical plan-view images 		Example Report »
		Chipworks E-Store »

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