



Intel® i5 660 Microprocessor 32 nm High-k Metal Gate CMOS Process

Structural Analysis Preliminary Table of Contents

For comments, questions, or more information about this report, or for any additional technical needs concerning semiconductor and electronics technology, please call Sales at Chipworks.

Structural Analysis – Preliminary Table of Contents

This preliminary Table of Contents is based on the previous generation Intel Xeon 45 nm Structural Analysis Report. It is provided to demonstrate the expected scope of this final report.



CHIPWORKS

www.chipworks.com



INSIDE • TECHNOLOGY

Structural Analysis – Preliminary Table of Contents

Table of Contents

Table of Contents

- 1 Overview**
 - 1.1 List of Figures
 - 1.2 List of Tables
 - 1.3 Company Profile
 - 1.4 Introduction
 - 1.5 Device Summary
 - 1.6 Process Summary

- 2 Device Overview**
 - 2.1 Package and Die
 - 2.2 Die Features

- 3 Die Utilization Analysis**
 - 3.1 Overview
 - 3.2 Functional Block Measurements

- 4 Selected Layout Feature Analysis**
 - 4.1 Metal 1 – Minimum Pitch and Dummy Metal Patterns
 - 4.2 Metal Gate Level – Transistor/Trench Contact Layout and Standard Logic Cells

- 5 Process Analysis**
 - 5.1 General Structure
 - 5.2 Dielectrics
 - 5.3 Metallization
 - 5.4 Vias and Contacts
 - 5.5 MOS Transistors
 - 5.6 Isolation
 - 5.7 Wells and Substrate

- 6 Embedded Memory Analysis**
 - 6.1 Embedded Memory Overview
 - 6.2 HD 6T SRAM Block and Cell Layout Analysis
 - 6.3 HD 6T SRAM Cross Section Analysis

- 7 Critical Dimensions**
 - 7.1 Functional Block Measurements
 - 7.2 Package Measurements
 - 7.3 Die Seal Via Widths
 - 7.4 Dielectric Thicknesses



Structural Analysis – Preliminary Table of Contents

- 7.5 Metallization Measurements
- 7.6 Via and Contact Measurements
- 7.7 MOS Transistor Measurements
- 7.8 Isolation Measurements
- 7.9 Wells and Substrate Measurements
- 7.10 HD 6T SRAM Transistor Sizes

8 References

- 8.1 Internet Links and Cited References
- 8.2 Related Chipworks Reports

9 Statement of Measurement Uncertainty and Scope Variation

About Chipworks



www.chipworks.com



1 Overview

1.1 List of Figures

2 Device Overview

- 2.1.1 E5410 Package Photograph – Top
- 2.1.2 E5410 Package Photograph – Bottom
- 2.1.3 Plan View Package X-Ray
- 2.1.4 Package Photograph – Top, IHS Removed
- 2.1.5 Die Photograph
- 2.1.6 Die Markings
- 2.1.7 Metal 1 Die Photograph – Analysis Sites
 - 2.2.1 Die Corner A
 - 2.2.2 Die Corner B
 - 2.2.3 Die Corner C
 - 2.2.4 Die Corner D
 - 2.2.5 Scribe Channel
 - 2.2.6 Large and Small Cu Die Bumps
 - 2.2.7 Cu Die Bumps – Tilt View
 - 2.2.8 Cu Die Bump Vias – TiltView

3 Die Utilization Analysis

- 3.1.1 Annotated Top Metal Die Photograph – Functional Blocks

4 Selected Layout Feature Analysis

- 4.1.1 Dummy Metal 1 Overview
- 4.1.2 Dummy Metal 1 – Standard Cells
- 4.1.3 Dummy Metal 1 Pitch
 - 4.1.4 Minimum Metal 1 Pitch (A)
 - 4.1.5 Minimum Metal 1 Pitch (B)
 - 4.1.6 Minimum Metal 1 Pitch (C)
- 4.2.1 Gate Layout – General Logic
- 4.2.2 Equivalent Minimum NAND Cell Size

5 Process Analysis

- 5.1.1 Penryn Die – General Structure
- 5.1.2 Die Thickness
- 5.1.3 Die Edge
- 5.1.4 Die Seal
- 5.1.5 Die Seal – Upper Level Via Width
- 5.1.6 Die Seal – Lower Level Via Width
- 5.2.1 Passivation
- 5.2.2 ILD 8 and ILD 7
- 5.2.3 ILD 6 – TEM
- 5.2.4 ILD 5 – TEM
- 5.2.5 ILD 4 – TEM
- 5.2.6 ILD 3 – TEM
- 5.2.7 ILD 2 – TEM



CHIPWORKS

www.chipworks.com



- 5.2.8 ILD 1 – TEM
- 5.2.9 PMD – TEM
- 5.2.10 Detail of PMD – TEM
- 5.2.11 TEM-EDS Spectrum of Passivation
- 5.2.12 TEM-EDS Spectrum of ILD 8
- 5.2.13 TEM-EDS Spectrum of ILD 7
- 5.2.14 TEM-EDS Spectrum of ILD 3
- 5.2.15 TEM-EDS Spectrum of PMD Upper Levels
- 5.2.16 TEM-EELS Spectrum of PMD 5
- 5.2.17 TEM-EELS Spectrum of PMD 4 (Gate Sealant)
- 5.2.18 TEM-EELS Spectrum of PMD 1 and PMD 3
- 5.2.19 TEM-EELS Spectrum of PMD 2 Contact Etch Stop Layer
- 5.2.20 TEM-EELS Spectrum of Gate Sidewall Spacer
- 5.3.1 Minimum Pitch Metal 9
- 5.3.2 Metal 9 Thickness
- 5.3.3 Metal 9 Barrier – TEM
- 5.3.4 Minimum Pitch Metal 8
- 5.3.5 Metal 7 Thickness – TEM
- 5.3.6 Minimum Pitch Metal 7 – TEM
- 5.3.7 Metal 6 Thickness
- 5.3.8 Metal 6 Composition – TEM
- 5.3.9 Minimum Pitch Metal 5 – TEM
- 5.3.10 Minimum Pitch Metal 4
- 5.3.11 Metal 4 Composition – TEM
- 5.3.12 Minimum Pitch Metal 3 – TEM
- 5.3.13 Metal 3 Liner – TEM
- 5.3.14 Minimum Pitch Metal 2
- 5.3.15 Metal 2 – TEM
- 5.3.16 Metal 2 Liner – TEM
- 5.3.17 Minimum Pitch Metal 1 – TEM
- 5.3.18 Metal 1 Thickness – TEM
- 5.3.19 Metal 1 Liner – TEM
- 5.3.20 TEM-EDS Spectra of Metal 9 Layers
- 5.3.21 TEM-EDS Spectrum of Metal 1 Liner
- 5.4.1 Cu Die Bump Via Pitch
- 5.4.2 Cu Die Bump Via Window
- 5.4.3 Minimum Pitch Via 8s
- 5.4.4 Minimum Pitch Via 7s and Minimum Width Via 8
- 5.4.5 Via 7 – TEM
- 5.4.6 Minimum Pitch Via 6s
- 5.4.7 Via 6 – TEM
- 5.4.8 Minimum Pitch Via 5s
- 5.4.9 Via 5 – TEM
- 5.4.10 Minimum Pitch Via 4s
- 5.4.11 Via 4 – TEM



- 5.4.12 Minimum Pitch Via 3s
- 5.4.13 Via 3 – TEM
- 5.4.14 Minimum Observed Pitch Via 2s
- 5.4.15 Via 2 – TEM
- 5.4.16 Round and Oval Via 1s
- 5.4.17 Narrow and Wide Via 1s
- 5.4.18 Minimum Pitch Via 1s
- 5.4.19 Via 1 – TEM
- 5.4.20 Minimum Pitch Contact Extensions
- 5.4.21 Metal 1/Contact Interface
- 5.4.22 Top of W M0 Trench Contact
- 5.4.23 Trench Contact Over STI
- 5.4.24 Gate Contact
- 5.4.25 Contact to N⁺ S/D Diffusion
- 5.4.26 Contact to P⁺ S/D Diffusion
- 5.4.27 Metal 0 Trench Contact Strap
- 5.4.28 TEM-EDS Spectrum of Metal 0 Liner
- 5.5.1 PMOS Transistor Overview – TEM
- 5.5.2 Stacking Fault in Embedded SiGe
- 5.5.3 Embedded SiGe Dimensions
- 5.5.4 PMOS Gate Dielectric and Work Function Metal
- 5.5.5 PMOS Transistor – Bottom of Gate Electrode
- 5.5.6 PMOS Gate SWS
- 5.5.7 Minimum Gate Length PMOS Core Logic Transistor
- 5.5.8 NMOS Transistor Overview
- 5.5.9 NMOS Gate Dielectric and Work Function Metal
- 5.5.10 NMOS Transistor – Bottom of Gate Electrode
- 5.5.11 NMOS Gate SWS
- 5.5.12 Minimum Gate Length NMOS Core Logic Transistor
- 5.5.13 NMOS and PMOS Shared Gate Finger – Longitudinal TEM Section
- 5.5.14 TEM-EDS Reference
- 5.5.15 TEM-EDS Spectrum of Substrate (A)
- 5.5.16 SiGe Analysis – Line Scan Reference
- 5.5.17 SiGe Filled Cavity, Si and Ge Concentration (B, Horizontal Scan)
- 5.5.18 SiGe Filled Cavity, Si and Ge Concentration (C, Vertical Scan)
- 5.5.19 TEM-EDS Spectrum of P⁺ S/D Silicide
- 5.5.20 TEM-EDS Spectrum of N⁺ S/D Silicide
- 5.5.21 TEM-EELS Spectrum of SiO₂ Gate Oxide (D)
- 5.5.22 TEM-EDS Spectrum of HfO₂ High-k from PMOS (E)
- 5.5.23 TEM-EDS Spectrum of HfO₂ High-k from NMOS (F)
- 5.5.24 TEM-EDS Spectrum of PMOS Work Function Metal (G)
- 5.5.25 TEM-EDS Spectrum of NMOS Work Function Metal (H)
- 5.5.26 TEM-EDS Spectrum of Ta-based Liner – Trench Sidewall
- 5.5.27 TEM-EDS Spectrum of TiN PMOS Trench Barrier (J)
- 5.5.28 TEM-EDS Spectrum of TiAl (54/46) Gate Fill (K)



- 5.5.29 TEM-EELS Spectrum of TiN Barrier in Trench Fill (L)
- 5.5.30 TEM-EDS of TiAl (45/55) Fill Above TiN Trench Barrier (M)
- 5.5.31 TEM-EDS Spectrum of TiAl (23/77) Gate Fill (N)
- 5.5.32 TEM-EDS Spectrum of Gate Capping Layer (O)
- 5.6.1 Minimum Width STI
- 5.6.2 STI Thickness Beneath PMOS Routing Metal
- 5.6.3 STI Gate Wrap (A)
- 5.6.4 STI Gate Wrap (B)
- 5.6.5 Minimum Width Si
- 5.7.1 SCM of N and P-Wells in HD 6T SRAM
- 5.7.2 SCM of N-Well and P-Epitaxial Layer
- 5.7.3 SRP of P-Well, P-Epi, and Substrate
- 5.7.4 SIMS Profile of N-Type Dopants
- 5.7.5 SIMS Profile of P-Type Dopant

6 Embedded Memory Analysis

- 6.1.1 6T SRAM Schematic
- 6.2.1 HD 6T SRAM – Metal 3, Block Corner
- 6.2.2 HD 6T SRAM – Metal 3, Intra Block Circuitry
- 6.2.3 HD 6T SRAM – Metal 2, Block Corner
- 6.2.4 HD 6T SRAM – Metal 2, Intra Block Circuitry
- 6.2.5 HD 6T SRAM – Metal 1, Block Corner (Right)
- 6.2.6 HD 6T SRAM – Metal 1, Intra-Block Circuitry
- 6.2.7 HD 6T SRAM – Gate Level, Partial Block Overview
- 6.2.8 HD 6T SRAM – Gate Level, Block Corner
- 6.2.9 HD 6T SRAM – Gate Level, Intra-Block Circuitry
- 6.2.10 HD 6T SRAM – Metal 3, Unit Cell
- 6.2.11 HD 6T SRAM – Metal 2, Unit Cell
- 6.2.12 HD 6T SRAM – Metal 1, Unit Cell
- 6.2.13 HD 6T SRAM – Gate Level, Unit Cell
- 6.2.14 HD 6T SRAM – Diffusion, Unit Cell
- 6.3.1 NMOS Access Gate Length
- 6.3.2 NMOS Pull-Down Gate Length
- 6.3.3 PMOS Pull-Up Gate Length
- 6.3.4 NMOS Access Transistors
- 6.3.5 NMOS Access Transistor Gate Width
- 6.3.6 PMOS Pull-Up and NMOS Pull-Down Gates
- 6.3.7 NMOS Pull-Down Transistor Gate Width
- 6.3.8 PMOS Pull-Up Transistor Gate Width



CHIPWORKS

www.chipworks.com



1.2 List of Tables

- 1 Overview**
 - 1.4.1 Device Identification (Sample 7)
 - 1.5.1 E5410 Device Summary
 - 1.6.1 Penryn Die Process Summary
- 2 Device Overview**
 - 2.1.1 Sample Identification and Analysis Record
- 3 Die Utilization Analysis**
 - 3.2.1 Die Utilization
- 5 Process Analysis**
 - 5.1.1 Die Seal Via Widths
 - 5.2.1 Dielectric Thicknesses
 - 5.3.1 Metallization – Vertical Dimensions
 - 5.3.2 Metallization – Horizontal Dimensions
 - 5.4.1 Via and Contact Observed Dimensions
 - 5.5.1 MOS Transistor Horizontal Dimensions
 - 5.5.2 MOS Transistor Vertical Dimensions
 - 5.5.3 Speculative Process Flow For Replacement Gates
 - 5.5.4 Transistor Materials Analysis Summary
 - 5.6.1 STI – Measured Dimensions
 - 5.7.1 Die Thickness and Well Depths
- 6 Embedded Memory Analysis**
 - 6.3.1 6T SRAM Transistor Sizes
- 7 Critical Dimensions**
 - 7.1.1 Die Utilization
 - 7.2.1 Observed Package Horizontal Dimensions
 - 7.2.2 Measured Package Thicknesses
 - 7.3.1 Die Seal Via Widths
 - 7.4.1 Dielectric Thicknesses
 - 7.5.1 Metallization – Vertical Dimensions
 - 7.5.2 Metallization – Horizontal Dimensions
 - 7.6.1 Via and Contact Observed Dimensions
 - 7.7.1 MOS Transistor Horizontal Dimensions
 - 7.7.2 MOS Transistor Vertical Dimensions
 - 7.8.1 STI – Measured Dimensions
 - 7.9.1 Die Thickness and Well Depths
 - 7.10.1 6T SRAM Transistor Sizes
- 8 References**
 - 8.2.1 Intel Microprocessors Analyzed by Chipworks



CHIPWORKS