Table of Contents	Description
1) Overview • Table of Contents • List of Figures and Tables • Introduction • Device Summary • Major Findings	• Device Summary is a very useful reference. • Typically used by TI for leading edge aCMOS, NAND and emerging memory only (note: used more widely by Patent Intelligence).
2) Device Overview • Package and Die • Die Features • Bond pads • Die corners	• Die features include memory blocks and unusual components • Image of partially delayered die, annotated with major functional blocks • Package cross-section not included (to be provide as separate PKG report) • SEM of standard logic cell, showing cell size
4) Process Analysis • SEM and TEM images • General Device Structure • Die seal including details • Bond Pads (including under bond pad) • Dielectrics • Metallization • Vias and Contacts • Transistors and Poly (core and peripheral; minimum gates, minimum contacted gates, minimum pitch poly) • Passive Components (if used) • Isolation (periphery and HD SRAM) • Wells and Substrate	• Chipworks methodology is Evidence based reporting • Use SEM and TEM images to show each feature. Images required of all dielectric levels, metal levels, transistors, poly and isolation. • Will include Bipolar and/or LDMOS transistors if present. • TEM required for isolation • SRP and/or SIMS dopant depth profile of Wells • SCM and/or SEM images of well structure may be included
5) Minimum Sized Memory Cell Analysis • Cell analysis - schematic • Cell Plan-View Analysis for minimum sized HD SRAM • Cell Cross-sectional Analysis Parallel to Bitline • Cell Cross-Sectional Analysis Parallel to Wordline (may be included, standard for memory devices)	• Included if device is a memory device or device has substantial embedded memory • Done for minimum sized SRAM memory on device • Plan-view images to show metal 3 down to diffusion at appropriate low and high magnification.
6) Materials Analysis • SEM-EDS Analysis of materials • TEM-EDS Analysis of Dielectrics, Metals and Gates • SIMS Analysis of Dielectrics (Optional)	• SEM and TEM-EDS determine elements of a material • Optional SIMS determines chemical composition for complex dielectric stacks when sufficient area is available • TEM-EDS of dielectrics used to supplement SIMS analysis for low-k dielectrics

7) Optional Layout and Topology Analysis • Annotated M1 or poly die photograph, showing the macro blocks • Die utilization table(s) showing the % area used by each macro block, if appropriate. Plus relevant die layout features including, as appropriate: • Layout under bond pads • Dummy metal patterns and dummy STI • Standard Logic at poly and/or M1 • Standard Logic Estimated Equivalent Gate Count Analysis • Memory blocks at high and low magnification (up to three types of memory, SRAM, Flash, DRAM, etc.) • Layout of device structures, such as bipolar transistors, DMOS transistors, resistors, caps, etc	• Included for advanced CMOS devices only • Selected detailed SEM and optical plan-view images, at low and high magnification of relevant features. • Optional *ICInside Surveyor* (ICS) deliverable will be offered. High resolution images for the fine pitch layer, typically poly, M1, M2 and M3 will be provided for an approximately 1 mm^2 area of the die. The area will be selected to sample standard logic, memory and I/O areas of the die, when possible.
8) Critical Dimensions • Horizontal Dimensions (metals, vias, transistors, poly, isolation, bond pads, memory cells) • Vertical Dimensions (dielectrics, metals, poly, diffusions and die)	• Summary table for quick access
Normal Scope of Lab Work	• Up to three (3) TEM cross-sections, including both gate oxides, if present. All relevant TEM images captured will be included in report. • Typically 4-6 SEM cross-sections, plus bevel of SRAM cell. • Delayered "poly" die.