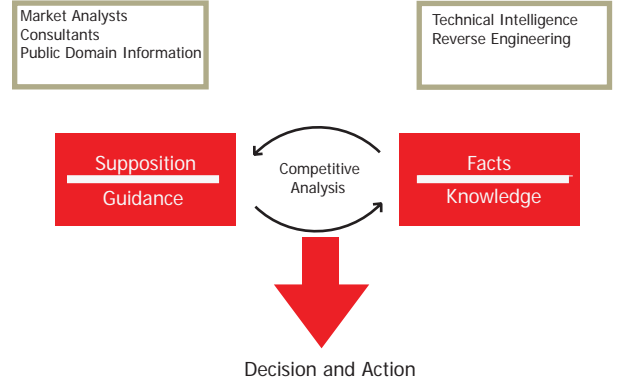


# Chipworks Functional Analysis Reports



Chipworks Functional Analysis Reports are designed to provide engineers, design managers, product line managers, and business unit managers with an assessment of the architectural innovations of their competitors' devices. Functional Analysis Reports answer questions with difficult to obtain information that complements other forms of competitive intelligence to, deliver the following key benefits to the client:

- 1) The first step in gathering technical intelligence about competing devices, for cost analysis and understanding of high-level innovation.
- 2) Easiest information to consume and use for decision making by the broadest possible audience within the receiving organization.
- 3) Fact-based analysis lets you make benchmarking decisions, such as whether to re-design IP blocks, use third party IP, shrink nodes, and set pricing.



## Types of Functional Analysis Reports

Basic	Standard	Advanced
Learn the node and quick examination of the layout. Used to scan broader market, and determine where further analysis is warranted.	Enables costing, but also an understanding of the architecture. Often used for a block-level analysis of where you are leading, and where you are falling behind.	Includes board-level identification of devices, in-depth discussion of the architecture of analog blocks not identified with public documentation, and I/O analysis.
<ul style="list-style-type: none"> <li>• Die photo</li> <li>• Lower metal sufficient to see architecture</li> <li>• Cross section</li> </ul>	<ul style="list-style-type: none"> <li>• Process summary</li> <li>• Package and die analysis</li> <li>• Process analysis (via SEM) and critical dimensions</li> <li>• Annotated MI floorplan with major blocks identified (using public information)</li> <li>• Analog block analysis with high resolution of individual blocks</li> <li>• Memory analysis of the ten largest memories</li> <li>• Standard cell measurements</li> </ul>	Standard plus: <ul style="list-style-type: none"> <li>• Identification of devices on board</li> <li>• Discussion and analysis of block function not identified by public documents</li> <li>• I/O analysis with zoomed-in images of I/Os</li> <li>• Average standard cell density and estimated gate count analysis</li> <li>• Identification of digital blocks (where possible)</li> <li>• IP vendors found on device (using public information)</li> </ul>

### Other Reports Available (partial list)

- Circuit Analysis Report – Hierarchical schematics of analog blocks and netlists of digital blocks, delivered in an interactive software format called the ICInside Browser.
- Power Distribution – A form of the Circuit Analysis Report that traces the power grid from the power pads throughout the die.
- Cost Analysis – Approximation based on assumptions of wafer fab, packaging, and testing costs using the process and block size. Clients are free to plugin their own costing figures to test the assumptions.
- Package Analysis Report – Deconstruction of the package through a combination of x-ray and cross-sectional SEM imaging.
- Process Analysis Report – Detailed analysis of the process, with contents specific to the device type. For advanced node devices, TEM-based



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At Chipworks, we find out what's inside technology - specifically, what's inside chips, devices, software, almost anything electronic you can think of. Whether you're involved in patent protection or litigation, researching your latest product design, or just trying to find out what the competition's up to, let Chipworks do the analysis for you. We have the expertise to take apart the product - or the patent - to discover its secrets. An internationally-recognized leader in patent portfolio management and technical competitive analysis, Chipworks is headquartered in Ottawa, Canada, with offices and representation worldwide.