

Table of Contents	Description
<p><b>1) Overview</b></p> <ul style="list-style-type: none"> <li>• Table of Contents</li> <li>• List of Tables and Figures</li> <li>• Introduction</li> <li>• Process Summary</li> </ul>	<p>The PNA report provides basic device information and is typically used to do simple cost estimates or to determine if the device warrants further analysis. The objective is to define node and process type (CMOS, BiCMOS, BCD, DMOS, etc).</p>
<p><b>2) Device Identification</b></p> <ul style="list-style-type: none"> <li>• Package and Die</li> <li>• Package photos and X-ray's</li> <li>• Die photo Top Metal</li> <li>• Die markings</li> <li>• Die corners</li> <li>• Bond pads</li> <li>• Die features</li> </ul>	<p>Device identification supplies the die images with identification markings (where available) at the top metal; along with basic device features.</p> <ul style="list-style-type: none"> <li>• Optical pictures of die features, including die corner, bond pads, plus bipolar transistors, inductors, etc., if present.</li> </ul>
<p><b>3) Process Analysis</b></p> <ul style="list-style-type: none"> <li>• SEM of General Device Structure</li> <li>• SEM of Minimum Metal 1</li> <li>• SEM of MOS transistor (technology node)</li> <li>• SEM of bipolar/DMOS (if no MOS present)</li> </ul>	<p>Basic analysis of the process using SEM images.</p> <ul style="list-style-type: none"> <li>• SEM image of general device structure</li> <li>• SEM image minimum M1, and MOS transistor (technology node)</li> <li>• Typically three SEM images (glass-etch SEM only for CMOS).</li> <li>• SEM image of bipolar or DMOS, if no MOS present (Si-etch).</li> </ul>
<p><b>Optional Analysis (additional cost)</b></p> <ul style="list-style-type: none"> <li>• Package X-Section</li> <li>• Additional SEM X-Section</li> <li>• Delayering and High Magnification Die Photo</li> <li>• Additional cost for process analysis, if part contains more than one die.</li> <li>• Optional Critical Dimensions (CD) Table for metal layers, poly layers, MOS transistor gates, contacts and isolation</li> </ul>	<ul style="list-style-type: none"> <li>• Annotated package cross section</li> <li>• Package wiring dimensions and vias</li> <li>• Package material construction</li> <li>• One Cross Section through specified area</li> <li>• Includes up to 4 SEM images for each X-section</li> <li>• Includes one die photo at resolution required for best fit on 8.5"X11" page. M1 or Polysilicon (please specify)</li> <li>• Same scope as 3) for each additional die.</li> </ul>

\* PNA replaces the CTR report format as at August 2007

Please note, due to the nature of reverse engineering, Chipworks report content may vary. Reports published prior to the latest revision date (Aug 2007) may contain different content than stated above.

