Table of Contents	Description
1) Overview • Table of Contents • List of Figures and Tables • Introduction • Major Findings	Device summary with an overview of the analysis. • Includes a table(s) of key measurements. Use this to quickly compare between reports. • Evidence-based analysis proves all conclusions with images.
2) Device Overview • Package and Die • Die Features	Reports are written from an “outside-in” approach. This section looks at the device features. • Die features include memory blocks, and unusual components
3) Process Analysis • SEM images • General Device Structure • Bond Pads • Dielectrics • Metallization • Vias and Contacts • Transistors and Poly • Passive Components (If used) • SRP of wells	The process analysis section provides critical information about the design, including: • SEM images showing each feature. • Images of all dielectric levels, metal levels, transistors, poly and isolation. • SCM is typically included (device dependent).
4) Memory Cell Analysis • Cell Plan-View Imaging • Cell Cross-sectional Imaging Parallel to Bitline	Memory is a critical component of many devices and processes. • Included if device is a memory device or device has substantial embedded memory. • Done for major memory types. • Plan-view images to show metal 3 down to diffusion.
5) Critical Dimensions • Horizontal Dimensions (metals, vias, transistors, poly, isolation, bond pads, memory cells) • Vertical Dimensions (dielectrics, metals, poly, diffusions, wells and die)	Full tabulation of all measurements taken in the analysis allows a detailed comparison between devices.
Optional (additional cost) • TEM images • SEM-EDS Analysis of Materials • TEM-EDS Analysis of Dielectrics, Metals and Gates • SIMS Analysis of Dielectrics	

Please note, due to the nature of reverse engineering, Chipworks report content may vary. Reports published prior to the latest revision date (May 2007) may contain different content than stated above.